Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A bipolar junction transistor (BJT) fabricated with a process having a minimum process dimension of X μm and a minimum alignment tolerance, comprising:

a semi-insulating substrate,

a subcollector formed on said substrate,

a collector formed on said subcollector,

a first metal contact on said subcollector which provides a collector contact for said BJT,

a base formed on said collector,

an emitter formed on said base,

a cross-shaped second metal contact on said emitter which provides an emitter contact for said BJT, said emitter contact comprising two perpendicular arms which intersect at a central area, the width of each of said arms being about equal to X μm;

an inter-level dielectric layer on said emitter contact; and

a via through said inter-level dielectric layer which provides access to said emitter contact, said via being square-shaped, centered over the center point of said central area, and oriented at a 45° angle to said arms such that said via can be sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact.

2. (canceled) The BJT of claim 1, wherein said fabrication process has a minimum alignment tolerance, said square-shaped via sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact.

3. (original) The BJT of claim 1, wherein said semi-insulating substrate comprises indium phosphide (InP).

4. (original) The BJT of claim 1, wherein said semi-insulating substrate is a compound semiconductor.

5. (original) The BJT of claim 1, wherein said arms are generally rectangular, have respective center points, are of approximately equal length, and intersect at their respective center points.

6. (original) The BJT of claim 1, wherein said sub-collector comprises indium phosphide (InP) or indium gallium arsenide (InGaAs).

7. (original) The BJT of claim 1, wherein said collector comprises indium phosphide (InP), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), or indium aluminum arsenide phosphide (InAlAsP).

8. (original) The BJT of claim 1, wherein said base comprises indium gallium arsenide (InGaAs).

9. (original) The BJT of claim 1, wherein said base comprises gallium arsenide antimonide (GaAsSB).

10. (original) The BJT of claim 1, wherein said emitter comprises indium phosphide (InP) or indium aluminum arsenide (InAlAs).

11. (original) The BJT of claim 1, wherein said semi-insulating substrate is a compound semiconductor and said BJT structure is arranged to form a heterojunction bipolar transistor (HBT).

12. (original) A heterojunction bipolar transistor (HBT) fabricated with a process having a minimum process dimension of X μm and a minimum alignment tolerance, comprising:

a semi-insulating substrate comprising a compound semiconductor;

a subcollector formed on said substrate;

a collector formed on said subcollector;

a first metal contact on said subcollector which provides a collector contact for said HBT;

a base formed on said collector;

an emitter formed on said base;

a cross-shaped second metal contact on said emitter which provides an emitter contact for said BJT, said emitter contact comprising two perpendicular arms which intersect at a central area, the width of each of said arms being about equal to X μm;

an inter-level dielectric layer on said emitter contact; and

a via through said inter-level dielectric layer which provides access to said emitter contact, said via being square-shaped, centered over the center point of said central area, and

oriented at a 45° angle to said arms, said square-shaped via sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact.

13. (original) The HBT of claim 12, wherein said semi-insulating substrate comprises indium phosphide (InP).

14. (original) The HBT of claim 12, wherein said arms are generally rectangular, have respective center points, are of approximately equal length, and intersect at their respective center points.

15. (original) The HBT of claim 12, wherein said sub-collector comprises indium phosphide (InP) or indium gallium arsenide (InGaAs).

16. (original) The HBT of claim 12, wherein said collector comprises indium phosphide (InP), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), or indium aluminum arsenide phosphide (InAlAsP).

17. (original) The HBT of claim 12, wherein said base comprises indium gallium arsenide (InGaAs).

18. (original) The HBT of claim 12, wherein said base comprises gallium arsenide antimonide (GaAsSb).

19. (original) The HBT of claim 12, wherein said emitter comprises indium phosphide (InP) or indium aluminum arsenide (InAlAs).